WHAT IS CLAIMED IS:

1. A semiconductor device formed on a semiconductor chip, comprising:

a circuit area including an electronic circuit disposed on a surface of the semiconductor chip;

a metal guard ring disposed on said surface of the semiconductor chip, surrounding the circuit area; and

a passivation layer covering said surface of the semiconductor chip, the passivation layer having a slot disposed above the metal guard ring, the slot extending down to the metal guard ring and surrounding the circuit area.

2. The semiconductor device of claim 1, wherein the metal guard ring has an inside edge and an outside edge, the slot is narrower than the metal guard ring, and the inside edge and the outside edge of the metal guard ring are covered by the passivation layer.

3. The semiconductor device of claim 2, wherein:

the semiconductor chip has a corner;

the metal guard ring has a slit disposed between said inside edge and said outside edge at least at said corner; and

the slot in the passivation layer avoids said slit, leaving said slit covered by the passivation layer.

4. The semiconductor device of claim 3, wherein the slot in the passivation layer is disposed between said slit and the outside edge of the metal guard ring.

5. A method of manufacturing a semiconductor device, comprising:

forming an electronic circuit with on a surface of a

semiconductor chip, and forming a metal guard ring surrounding the electronic circuit on said surface of the semiconductor chip;

covering said surface of the semiconductor chip, including the electronic circuit and the metal guard ring, with a passivation layer; and

forming a slot in the passivation layer above the metal guard ring, the slot extending down to the metal guard ring and surrounding the electronic circuit.

6. The method of claim 5, wherein:

the forming of said electronic circuit includes forming a metal pad within the electronic circuit; and

the forming of said slot includes simultaneously forming an opening in the passivation layer above the metal pad, for connection of a bonding wire to the metal pad.

7. The method of claim 5, wherein the metal guard ring has an inside edge and an outside edge, the slot is narrower than the metal guard ring, and the inside edge and the outside edge of the metal guard ring are covered by the passivation layer.

8. The method of claim 7, wherein:

the semiconductor chip has a corner;

the metal guard ring has a slit disposed between said inside edge and said outside edge at least at said corner; and

the slot in the passivation layer avoids said slit, leaving said slit covered by the passivation layer.

9. The method of claim 8, wherein the slot in the passivation layer is disposed between said slit and the outside edge of the metal guard ring.